Amendments to the Claims:

This listing will replace all prior versions, and listing, of claims in the application.

1. (currently amended) A method for monitoring electron charge effect occurring during semiconductor processing, comprising ~~the steps of~~:

providing a substrate, a layer of n-type conductivity having been created in said substrate;

creating a pattern of Local Oxidation of Silicon (LOCOS) regions in said substrate, said pattern of LOCOS being interspersed with exposed regions of said substrate;

etching said exposed regions of said substrate using said pattern of LOCOS regions as a hard mask, creating a pattern of elevated LOCOS regions, creating trenches having inside surfaces in said substrate;

creating a layer of interlayer oxide over said pattern of LOCOS regions and said inside surfaces of said trenches created in said substrate;

depositing [[a]] said layer of polysilicon over said layer of interlayer oxide;

patterning said layer of polysilicon, said patterned layer of polysilicon comprising at least one contact point over said substrate, completing creation of a electron charge monitoring device having a surface;

providing a semiconductor processing tool, said semiconductor processing tool being designated as being a tool being evaluated for electron charge effect of a process being performed by said tool;

positioning said substrate comprising said electron charge monitoring device inside said processing tool in a location and a position ~~being identical with a position and location~~ being occupied by a substrate being processed by said tool;

establishing processing conditions of a process as these processing conditions apply for said process and said tool;

exposing said electron charge monitoring device to said established processing conditions for a period of time ~~having a measurable duration~~;

terminating said processing conditions;

removing said electron charge monitoring device from said semiconductor processing tool; and

measuring a voltage required to induce a FN tunneling based current between the at least one contact point of said patterned layer of polysilicon and said substrate.

2. (previously presented) The method of claim 1, said creating a pattern of Local Oxidation of Silicon (LOCOS) regions in said substrate comprising the steps of:

depositing a layer of silicon nitride over said substrate;

patterning said layer of silicon nitride, creating a mask of silicon nitride over said substrate, elements of said mask being interspersed with exposed regions of said substrate;

creating layers of Local Oxidation of Silicon (LOCOS) in said exposed regions of said substrate; and

removing said mask of silicon nitride from said substrate.

3. (previously presented) The method of claim 1, wherein said layer of interlayer oxide is HTO, dry oxide or wet oxide.

4. (original) The method of claim 1, said layer of interlayer oxide being created to a thickness between about 80 and 300 Angstrom.

5. (currently amended) The method of claim 1, said layer of polysilicon being deposited to a thickness within the range of between about 1,500 and 6,000 Angstrom.

Claims 6-11: (cancelled)

12. (currently amended) The method of claim 1, said current induced between said layer of polysilicon and said substrate being about 0.1 μA.

13. (currently amended) A method of creating an electron charge effect monitoring device, comprising the steps of:

providing a substrate, a layer of n-type conductivity having been created in said substrate;

creating a pattern of Local Oxidation of Silicon (LOCOS) regions in said substrate, said pattern of LOCOS being interspersed with exposed regions of said substrate;

etching said exposed regions of said substrate using said pattern of LOCOS regions as a hard mask, creating a pattern of elevated LOCOS regions, creating trenches having inside surfaces in said substrate;

creating a layer of interlayer oxide over said pattern of LOCOS regions and said inside surfaces of said trenches created in said substrate;

depositing [[a]] said layer of polysilicon over said layer of interlayer oxide;

patterning said layer of polysilicon, said patterned layer of polysilicon comprising at least one contact point over said substrate; and

measuring a voltage required to induce a FN tunneling based current between said at least one contact point of said patterned layer of polysilicon and said substrate after said substrate has been exposed to a semiconductor processing tool under known conditions of processing by said semiconductor processing tool.

14. (previously presented) The method of claim 13, said creating a pattern of Local Oxidation of Silicon (LOCOS) regions in said substrate comprising the steps of:

depositing a layer of silicon nitride over said substrate;

patterning said layer of silicon nitride, creating a mask of silicon nitride over said substrate, elements of said mask being interspersed with exposed regions of said substrate;

creating layers of Local Oxidation of Silicon (LOCOS) in said exposed regions of said substrate; and

removing said mask of silicon nitride from said substrate.

15. (previously presented) The method of claim 13, wherein said layer of interlayer oxide is HTO, dry oxide or wet oxide.

16. (original) The method of claim 13, said layer of interlayer oxide being created to a thickness between about 80 and 300 Angstrom.

17. (currently amended) The method of claim 13, said layer of polysilicon being deposited to a thickness within the range of between about 1,500 and 6,000 Angstrom.

Claims 18-22: (cancelled).

23. (previously presented) The method of claim 13, whereby said electron charge effect monitoring device can be recycled by applying an additional step of thermally annealing said substrate, thereby thermally annealing said electron charge monitoring device having been created in and on said substrate.

Claims 24-32: (cancelled).

Please enter the following new claims:

33. A method for monitoring electron charge effect occurring during semiconductor processing, comprising:

forming a monitor wafer having floating gate structures;

exposing the monitor wafer to a plasma process; and

measuring plasma damage by measuring interlayer oxide electron trap out rate.

34. The method of claim 33, said measuring interlayer oxide electron trap out rate comprising measuring a voltage required to induce a FN tunneling based current between at least one contact point of said floating gate structures and said monitor wafer.

35. The method of claim 34, said FN tunneling based current between at least one contact point of said floating gate structures and said monitor wafer being about 0.1 μA.